

WHAT IS CLAIMED IS:

- Muba7*
1. A semiconductor integrated circuit device comprising:
 - an internal circuit whose state of operation is controlled in response to an internal operation control signal; and
 - a control circuit for forming the internal operation control signal,

wherein said control circuit has its inputs connected to a terminal to which an external operation control signal is supplied and a terminal to which a timing signal used exclusively for testing is supplied, said control circuit being capable of providing control between a test mode and a normal operation mode,

wherein, in the test mode, the internal operation control signal is changed from a first state of control to a second state of control in response to a change of the external operation control signal from a first state to a second state, and the internal operation control signal is changed to the first state of control in response to the timing exclusively used for testing, and

wherein, in the normal operation mode, the internal operation control signal is changed from the first state of control to the second state of control in response to the change of the external operation control signal from the first state to the second state, and the internal operation control signal is

- 55 -

changed to the first state of control in response to the change of the external operation control signal to the first state.

2. A semiconductor integrated circuit device according to claim 1, wherein the external operation control signal consists of a plurality of control signals, and the first state and the second state are defined by a combination of levels of the plurality of control signals.

3. A semiconductor integrated circuit device according to claim 2, wherein said internal circuit is a memory circuit, the plurality of control signals consist of a memory select signal and a clock signal, and the internal operation control signal is changed from the first state of control to the second state of control in response to the change to a first level of the memory select signal fetched in synchronism with the clock signal, and is changed to the first state of control by a signal corresponding to a second level of the memory select signal synchronized with the clock signal.

4. A semiconductor integrated circuit device according to claim 3, wherein said memory circuit includes a memory cell which has its selection terminal connected to a corresponding word line and its data terminal connected to a corresponding bit line, and said memory circuit effects the sequential operation of the operation of terminating the word line selection in

- 56 -

correspondence with the first state of control of the internal operation control signal and of the operation of resetting the potential at the bit line to a predetermined level.

5. A semiconductor integrated circuit device according to claim 3, wherein said memory circuit includes a read/write memory cell which has its selection terminal connected to a corresponding word line and its data terminal connected to a corresponding bit line, starts the word line selection in response to the change of the internal operation control signal from the first state of control to the second state of control, and terminates the word line selection in response to the change of the internal operation control signal to the first state of control, and wherein the sequential operation of the operation of starting the word line selection and of the operation of imparting write data into the bit line for the write operation of data is effected in response to the change of the internal operation control signal from the first state of control to the second state of control.

6. A semiconductor integrated circuit device according to claim 1, wherein said terminal to which the timing signal used exclusively for testing is supplied is a terminal provided on a semiconductor integrated circuit chip as a terminal used exclusively for the timing signal used exclusively for testing.

7. A semiconductor integrated circuit device

- 57 -

according to claim 1, wherein said control circuit has an input to which a mode signal is supplied, and effects the control operation in the test mode and the control operation in the normal operation mode in response to the mode signal.

8. A semiconductor integrated circuit device according to claim 1, wherein the clock signal is set as a clock signal of a frequency lower than that at the time of the normal operation in correspondence with the performance of a testing apparatus in the test mode, and a phase difference of the timing signal for testing with the clock signal forms an internal operation control signal corresponding to the frequency of the clock signal at the time of the normal operation.

9. A method of testing a memory circuit which has a plurality of signal nodes to which an operation control signal for controlling memory selecting operation and an operation timing signal are supplied, and in which word-line selecting operation, sense amplifier operation following the word-line selecting operation, memory selecting operation including data transmitting operation, and the termination of the memory selecting operation including the termination of the word-line selecting operation are effected on the basis of the operation control signal, a reference timing of the internal operation of said memory circuit being set by the operation timing signal, comprising the steps of:

- 58 -

lowering a frequency of the timing signal at the time of test operation by a testing apparatus to a level lower than at the time of normal memory operation in correspondence with the performance of said testing apparatus; and

changing a period of operation by the operation control signal by combining the timing signal at the time of the test operation with a timing signal used exclusively for testing so as to test response characteristics of said memory circuit.

10. A method of testing according to claim 9, wherein said memory circuit has read/write memory cells, and effects the memory selecting operation including the word-line selecting operation based on the operation control signal and the operation of writing data into said memory cell selected by the word-line selecting operation, and wherein the period of operation of said memory circuit is changed by changing an input timing of the timing signal used exclusively for testing with respect to the timing signal, and the data write response characteristics of said memory circuit are tested on the basis of the change of the period of operation.

11. A method of testing according to claim 9, wherein upon termination of the memory selecting operation said memory circuit effects sequential operation including the termination of the word-line selecting operation and the reset operation for

- 59 -

resetting to a predetermined level the potential of a bit line to which data for a memory cell is imparted, and a period up to a change timing of the operation control signal for starting next memory selecting operation is changed by changing an input timing of the timing signal used exclusively for testing, so as to test the response characteristics of the reset operation.

12. A method of manufacturing a memory circuit which has a plurality of signal nodes to which an operation control signal for controlling memory selecting operation and an operation timing signal are supplied, and in which word-line selecting operation, sense amplifier operation following the word-line selecting operation, memory selecting operation including data transmitting operation, and the termination of the memory selecting operation including the termination of the word-line selecting operation are effected on the basis of the operation control signal, a reference timing of the internal operation of said memory circuit being set by the operation timing signal, said memory circuit having a defect remedy circuit, comprising:

a first step of preparing a semiconductor integrated circuit substrate on which said memory circuit and said defect remedy circuit are formed;

a second step of testing response characteristics of said memory circuit by a testing

- 60 -

apparatus by setting a frequency of the timing signal to a level lower than that at the time of normal operation in correspondence with the performance of said testing apparatus, by controlling a period of operation of said memory circuit through a combination of the timing signal and a timing signal used exclusively for testing, and by controlling the period of operation;

a third step of determining a portion of said memory circuit whose defect is to be remedied on the basis of a result of the testing of the response characteristics; and

a fourth step of remedying by said defect remedy circuit the portion whose defect is to be remedied and which has been determined in the third step.